Paper No. 27

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FRANK R. BRYANT

Appeal No. 1998-1439
Application 08/159,461

ON BRIEF

Before KRASS, LALL and GROSS, Administrative Patent Judges.

LALL, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the Examiner's final rejection[1] of claims 1-16, 24, 26-45, and 56. Claims 17-23, 25, 46-55, and 57 are withdrawn from consideration.

The invention relates to a method of forming an improved transistor gate structure. The process involves forming a nitride layer between a gate oxide layer and a polysilicon layer in a device region of a substrate isolated by field oxide regions. In the fabrication of

[1] An amendment after final was filed as Paper No. 17. However, there was no amendment made to the claims.

transistors on the order of 1.2 to 5 microns, reoxidation of an oxide/polysilicon gate structure is frequently utilized to improve transistor lifetimes and gate reliability. For submicron transistors, however, reoxidation degrades rather than improves transistor lifetimes, resulting primarily from the formation of asperities--small protrusions into the underlying layer--on the underside of the polysilicon layer by oxidant diffusion along polysilicon grain boundaries and polysilicon grain boundary slip. The nitride layer between the gate oxide and polysilicon electrode prevents oxidation of the bottom surface of the polysilicon as well as the grain boundary slip which results in the formation of asperities in submicron transistors. Reoxidatioin may thus be successfully utilized to extend transistor lifetimes. The nitride layer may be formed by directly depositing a nitride layer on the oxide prior to the deposition of the polysilicon, or by implanting nitrogen through the polysilicon and annealing the device to form a thin nitride layer. Claim 1 below further illustrates the invention.

1. A method for fabricating a portion of a semiconductor device comprising:

forming a gate structure on a substrate, the gate structure including an insulating oxide layer, a nitride layer and a polysilicon layer, wherein the oxide layer is located on the substrate, the nitride layer is located on the oxide layer, and the polysilicon layer is located on the nitride layer; and

reoxidizing the gate structure to form a layer of oxide over the gate structure.

The Examiner relies on the following references:

Geipel Jr. et al. (Geipel)	4,329,773	May 18, 1982
Haddad et al. (Haddad)	4,774,197	Sept. 27, 1988
Tsubone	5,100,820	Mar. 31, 1992

Wolf et al. (Wolf), Silicon Processing For The VLSI ERA, "Process Technology", Lattice Press, Vol. 1, pages 57-58, 307-308 (1986).

Claims 1-4, 6-7, 9-12, 14-15, 24[2], 26-32, 34-37, 39-44, and 56 stand rejected under 35 U.S.C. § 103 as being obvious over Geipel and Haddad, claims 5, 13, and 38[3] over Geipel, Haddad and Wolf, and claims 8, 16, 33, and 45 over Geipel, Haddad and Tsubone.

Rather than repeat the arguments of Appellant and the Examiner, we make reference to the briefs and the answer for the respective details thereof.

OPINION

We have considered the rejections advanced by the Examiner and the supporting arguments. We have, likewise, reviewed the Appellant's arguments set forth in the briefs[4].

We affirm.

In our analysis, we are guided by the general proposition that in an appeal involving a rejection under 35 U.S.C. § 103, an Examiner is under a burden to make out a prima facie

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[2] The Examiner withdrew the final rejection of claim 24 based on double patenting, in the Advisory Action (Paper No. 18), leaving only the rejection under 35 U.S.C. § 103.

[3] We note that claim 38 was omitted from the Examiner's statement of the rejection. However, claim is similar to claims 5 and 13. Therefore, we have included here claim 38 with claims 5 and 13.

[4] A reply brief was filed as Paper No. 25 on February 12, 1998 and is made of record.

case of obviousness. If that burden is met, the burden of going forward then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness, is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976). We are further guided by the precedent of our reviewing court that the limitations from the disclosure are not to be imported into the claims. In re Lundberg, 244 F.2d 543, 113 USPQ 530 (CCPA 1957); In re Queener, 796 F.2d 461, 230 USPQ 438 (Fed. Cir. 1986). We also note that the arguments not made separately for any individual claim or claims are considered waived. See 37 CFR § 1.192(a) and (c). In re Baxter Travenol Labs., 952 F.2d 388, 391, 21 USPQ2d 1281, 1285 (Fed. Cir. 1991) ("It is not the function of this court to examine the claims in greater detail than argued by an Appellant, looking for nonobviousness distinctions over the prior art."); In re Wiechert, 370 F.2d 927, 936, 152 USPQ 247, 254 (CCPA 1967)("This court has uniformly followed the sound rule that an issue raised below which is not argued in that court, even of it has been properly brought here by reason of appeal is regarded as abandoned and will not be considered. It is our function as a court to decide disputed issues, not to create them.").

ANALYSIS

At the outset, we note that according to Appellant, brief at pages 5-6, claims

1-16, 24, 26-45, and 56 are grouped as Group A and claims 5 and 13 are grouped as Group B.

We take claim 1 as the representative claim of Group A. The Examiner asserts, answer at pages 4 and 5, that Geipel shows everything except that it lacks anticipation [sic, teaching] of implanting nitrogen ions to form an oxide/nitride dual dielectric layer. The Examiner asserts, answer at page 5, that "it would have been obvious ... at the time of the invention to implant the silicon oxide gate dielectric in the known method of Geipel, Jr. with nitrogen ions as taught by Haddad et al. because this will prevent the inclusion of impurities into the gate oxide which will degrade its quality and overall lifetime." Appellant contends, brief, page 12 and reply brief, pages 3 and 4, that Haddad does not teach this process as forming a nitride layer between the oxide and the polysilicon, but rather as merely forming silicon nitride compounds within the oxide. The Examiner responds, page 7 of the answer, that, with respect to Haddad, the process used to form what Appellant calls "silicon-nitride compounds" within the gate oxide is an analogous process to that used in Appellant's invention. The examiner continues, "For instance, page 9 of Appellant's specification clearly states that when nitrogen implantation is used to form a silicon nitride layer, polysilicon layer 22 is deposited over oxide layer 16 as illustrated in Figure 9. Thereafter, nitrogen ions are implanted into transistor 10 as illustrated in Figure 10.... This is an analogous process including the same dosage range that is used in Haddad et al. reference. Therefore, it is clear that the silicon nitride compounds in Haddad can be

considered as silicon nitride layer in the same way applicant's invention is a silicon nitride layer."

We agree with the Examiner's interpretation of the word "layer" in the claim because the specification does not particularly delineate the term "layer" as used in the claim. Neither is there any recitation of the composition of the claimed layer. We also note that only a single passing reference is made by Appellant, brief at page 12, as to what Tsubone teaches and how Tsubone does not teach the use of the nitride layer between the oxide and polysilicon elements of the gate structure; however, Tsubone is not specifically argued relating to any particular claim.

Appellant further argues, brief at page 13, that "[a]t best, the proposed motivation for combining the teachings of Geipel, Jr. et al. with Haddad et al. constitutes a statement of why the combination is obvious to try. Nothing in those references suggests a reasonable expectation of success." We disagree with Appellant. Here, both Geipel and Haddad are concerned with the forming of similar electronic components, gate sources and drains, by making use of a silicon substrate. Haddad further discloses the improvement in the durability of such electronic components by the injection of nitrogen into the oxide layer. Therefore, in our view, the suggested combination of references is justified because it has been well settled while there must be some teaching, reason, suggestion, or motivation to combine existing elements to produce the claimed device, it is not necessary that the cited references or prior art specifically suggest making the combination (see B.F. Goodrich Co. v. Aircraft Braking Sys. Corp., 72 F.3d 1577, 1583, 37 USPQ2d 1314, 1319 (Fed. Cir. 1996)

and In re Nilssen, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988)) as Appellant would apparently have us believe. Rather, the test for obviousness is what the combined teachings of the references would have suggested to one of ordinary skill in the art. See In re Young, 927 F.2d 588, 591, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991) and In re Keller, 642 F.2d 413, 415, 208 USPQ 871, 881 (CCPA 1981). Moreover, in evaluating such references it is proper to take into account not only the specific teachings of the references but also the inferences which one skilled in the art would reasonably be expected to draw therefrom. In re Preda, 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968).

Consequently, we sustain the rejection of claims of Group A, i.e., claims 1-16, 24, 26-45, and 56 under 35 U.S.C. § 103.

GROUP B

The Examiner asserts, answer at page 6, that "it would have been obvious ... to substitute the nitrogen anneal [process] in the primary reference of Geipel, Jr. with a rapid thermal annealing process of approximately one thousand celsius for ten seconds as disclosed by Wolf et al. because this will minimize source/drain dopant diffusion and allow for high throughput (see page 58, second paragraph, last two lines)."

Appellant argues, brief at page 14, that "there is no basis for supposing that one skilled in the art would select rapid thermal annealing, which avoids redistribution of impurities, to perform an annealing step intended to redistribute implanted nitrogen." We again disagree with Appellant. We find that Wolf clearly teaches the process of rapid

thermal annealing in the fabrication of electronic components, see page 57 bottom paragraph. We agree with the Examiner that an artisan in the art of fabrication of silicon dioxide electronic components would have been concerned with the introduction of unwanted impurities in the formation of the electronic components. Therefore, a process such as rapid thermal annealing would have been a desirable process to be used in the implantation of nitrogen ions in the creation of sources, drains and gates on a silicon wafer. As we stated earlier, an explicit and specific teaching of the suggested combination is not required within the meaning of obviousness under 35 U.S.C. § 103. Therefore, we sustain the obviousness rejection of claims 5 and 13 over Geipel, Haddad and Wolf.

In conclusion, we sustain the obviousness rejection of claims 1-4, 6, 7, 9-12, 14, 15, 24, 26-32, 34-37, 39-44, and 56 over Geipel and Haddad. We also sustain the obviousness rejection of claims 5, 13, and 38 over Geipel, Haddad and Wolf, and of claims 8, 16, 33, and 45 over Geipel, Haddad and Tsubone.

The decision of the Examiner rejecting claims 1-16, 24, 26-45, and 56 under 35 U.S.C. § 103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

Errol A. Krass Administrative Patent Judge	)
Parshotam S. Lall Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
Anita Pellman Gross Administrative Patent Judge	)

PSL/cam

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